Remarks

Following the above amendments, claims 1, 4-8, 16, and 19-23 are pending in this application. By the amendments set out above, claim 17 has been cancelled. Claims 2, 3, 9-15, 18, and 24-27 were cancelled previously.

The remaining claims, including remaining independent claims 1, 16, and 22, have each been finally rejected under 35 U.S.C. § 103(a) as being obvious over the combination of Tyner et al. (U.S. Patent No. 6,272,618) or Goodman et al. (U.S. Patent No. 6,282,601) in view of Smith et al. (U.S. Patent No. 3,643,227) or Inoue (U.S. Patent No. 4,954,945).

A. Amendments to Independent Claims 1, 16, and 22

Each of independent claims 1, 16, and 22 has been amended herein to include the limitation that *each processor* of the computer system is operable to process a system management interrupt. Thus, each processor of the claimed multiple processor computer system is eligible to handle a system management interrupt. This invention stands in plain contrast to the teachings of both Goodman and Tyner.

The claimed invention is not obvious in view of any combination of the asserted prior art. Indeed, the only reference asserted by the examiner that discloses the concept of a computer system in which a processor is operable to handle a system management interrupt — Goodman — specifies that *all* system management interrupts will be handled by a *dedicated* processor. As such, the only prior art reference cited by the examiner that discloses the handling of a system management interrupt teaches that all system management interrupts are to be handled by a dedicated processor.

Applicants submit that a prima facie case of obviousness has not been established and that a rejection of the pending claims on obviousness grounds is improper. A prima facie

case of obviousness requires a showing that all of the claim limitations of the rejected claims are taught or suggested by the prior art. Manual of Patent Examining Procedure 2143 and 2143.03. The establishment of a prima facie case of obviousness requires that *all* the claim limitations be taught or suggested by the prior art. MPEP 2143.01 (emphasis added). "All words of a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (CCPA 1970). Here, because all of the elements of the independent claims, including the ability of the computer system to select among each of the processors of the computer system for the handling of the system management interrupt, are not taught or suggested by the prior art combination identified by the examiner, a prima facie case of obviousness cannot be established and the rejection of these claims should be withdrawn.

1. Goodman

Goodman does not disclose selecting a processor for handling the system management interrupt from a set of capable processors that include each processor of the computer system. Goodman, in contrast, specifies that all system management interrupts will be handled by a single, dedicated processor. Goodman carefully and clearly explains that "only the boot processor" (processor 12a of Figure 1 of Goodman) is able to serve as the system management interrupt handler:

> Although each of the processors 12 accepts the SMI, only the boot processor (e.g., system processor 12a) executes an SMI handler to service the SMI . . . .

(Goodman, column 4, lines 56-58). Goodman does not disclose or even suggest a method for handling system management interrupts in which a selection is made among the multiple processors that are operable to handle the system management interrupt. In Goodman, "only the boot processor" can handle the system management interrupt. Thus, it is plain from Goodman

that only one processor of Goodman — the dedicated boot processor — can handle the system management interrupt.

The claimed invention is patentably distinct from Goodman and the remainder of the cited prior art. The claimed invention is directed to a technique in which each processor of the computer system is operable to handle a system management interrupt. This element of the claimed invention is not disclosed or suggested by the prior art.

2. Tyner

Tyner describes a multiprocessor computer system wherein the computer performs a "find processor" routine to determine which processor caused the interrupt. (*See* Tyner at col. 4, line 29-34, Figure 2 and step 120). Applicants respectfully submit that the examiner is incorrect in his assertion that the "find processor" routine (step 120) of Tyner is used for the purpose of selecting a processor for the handling of the system management interrupt. The "find processor" routine of Tyner is not used for selecting a processor for the handling of a system management interrupt; the "find processor" routine of Tyner locates the processor that caused the system management interrupt:

> "[E]xecution proceeds to 120 where the computer performs a FIND PROCESSOR routine. The FIND PROCESSOR routine 120 determines which processor (12a or 12b) *caused* the SMI.

(Tyner, column 4, lines 31-34) (emphasis added). A plain reading of Tyner reveals that the "find processor" routine of Tyner is not involved in locating a processor to handle the system management interrupt. Rather, this routine identifies the processor that issues ("caused") the system management interrupt. Like Goodman, Tyner does not disclose a method for selecting a processor for handling a system management interrupt from one of the processors of the computer system.

3. Smith and Inoue

The Examiner recognizes that "[n]either Tyner nor Goodman explicitly discloses or teaches selecting a designated SMI processor according to an arbitration scheme. As described above, applicants respectfully submit that it should also be recognized that neither Tyner nor Goodman discloses or teaches selecting a processor for the handling of a system management interrupt from among a set of processors operable to handle a system management interrupt. Neither Smith nor Inoue cures this deficiency. Neither Smith nor Inoue in any manner concerns system management interrupts or a computer system in which multiple processors are each able to handle a system management interrupt.

4. Goodman Teaches Away From the Claimed Invention

There is no suggestion within the asserted prior art for modifying Goodman or Tyner to include the step of selecting from among multiple processors that are each operable to handle a system management interrupt.[1] Goodman expressly provides that all system management interrupts are to be handled by a *single, dedicated* processor. Considering Goodman's express teaching that "only the boot processor" is operable to handle a system management interrupt (column 4, line 57), Goodman itself teaches away from the combination suggested by the examiners, rendering the combination of Goodman and either Smith or Inoue impermissible.

It is improper to combine references that teach away from their combination. *In re Grasselli*, 713 F.2d 731 (Fed. Cir. 1983). MPEP 2145. Here, Goodman plainly discloses that "only the boot processor" is to be involved in handling the system management interrupt. A

[1] Tyner is not discussed in this Section A.4, as it is plain from the discussion above that the Examiner has misunderstood Tyner. Aside from the misunderstood and misquoted portion of Tyner (step 120 at column 4, lines 31-34), the Examiner has not identified any teaching in Tyner in which a processor is selected for the handling of a system management interrupt.

reference teaches away from the invention when a person of ordinary skill in the art, upon reading the reference, would be led in a path that is divergent from the path of the patent applicant. *See Tec Air, Inc. v. Denso Mfg. Mich. Inc.*, 192 F.3d 1353 (Fed. Cir. 1999). Here, there is no teaching to suggest from Goodman that any processor *other than* the boot processor is operable to handle a system management interrupt. From a plain reading of Goodman, a person of ordinary skill would be left with the conclusion that only a single, designated processor may be designated as the processor responsible for handling a system management interrupt. Applicants respectfully submit that a reading of Goodman cannot leave one with the teaching or suggestion that a processor for handling an issued system management interrupt can be selected from each of the processors of the computer system. Neither Smith nor Inoue supplies any teaching to the contrary; specifically, neither Smith nor Inoue supplies any teaching that each processor of a multiprocessor computer system is operable to handle a system management interrupt.

Modifying Goodman such that multiple processors of the modified reference are able to handle the system management interrupt would result in distortion of Goodman that is contrary to the teachings of Goodman and necessarily raises the impermissible use of hindsight reasoning on the part of the patent examiner. Nowhere does Goodman suggest that multiple processors could be used to handle system management interrupts. To the contrary, Goodman states that "only the boot processor" is to be used for that task. Goodman thus necessarily includes a well-developed teaching ("only the boot processor") that is directly contrary to the claimed invention, which involves a selection among multiple processors operable to handle a system management interrupt.

Any modification of Goodman to provide for a computer system in which each processor is operable to handle a system management interrupt would be contrary to the plain and persuasive teachings of Goodman. Goodman, therefore, cannot serve as a basis for a prima facie case of obviousness for the amended claims, and any combination of Goodman with Smith or Inoue for the sake of an obviousness rejection is impermissible. *See* MPEP 2145 (discussing in Parts X.A. and X.D. the inability of using hindsight to combine references or using those references that teach away from the proposed combination).

Applicants respectfully submit that the combination of Goodman, Tyner, Smith, and Inoue do not disclose or suggest invention of the amended claims of the present application, including the limitation of each of the independent claims directed to a selecting step in which the selection is made from a set of processors operable to handle the system management interrupt. Applicants request that the rejection of these claims on obviousness grounds be withdrawn.

B. Dependent claims 4-8, 19, and 23

Dependent claims 4-8, 19, and 23 will not be discussed individually herein, as each of these claims depends, either directly or indirectly, from an otherwise allowable base claim.

Conclusion

Applicants respectfully submit that the pending claims 1, 4-8, 16, and 19-23 of the present invention, as amended, are allowable. Applicants respectfully request that the rejection of the pending claims be withdrawn and that these claims be passed to issuance.

Respectfully submitted,

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